TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. 356202/00

In Re Application Of: **Ishiwata, et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/988,322	**November 19, 2001**	**Hung T. Vy**	**2828**

Invention:

AUTO POWER CONTROL CIRCUIT FOR LASER DIODE

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **February 26, 2004.**

The fee for filing this Appeal Brief is: **$330.00**

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Signature

Dated: **April 26, 2004**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

Ishiwata et al.

Serial No.: 09/988,322 Group Art Unit: 2828

Filed: November 19, 2001 Examiner: Vy, Hung T.

For: AUTO POWER CONTROL CIRCUIT FOR LASER DIODE

APPELLANTS' BRIEF ON APPEAL

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Appellants respectfully appeal the rejection of claims 1-22 in the Office Action dated November 27, 2003, as modified by the Interview Summary mailed March 1, 2004, to remove the rejection under 35 USC §112, second paragraph. A Notice of Appeal was timely filed on February 26, 2004. Filed concurrently herewith is a Petition to Admit Entry of Amendment Filed Under 37 CFR §1.116.

I. REAL PARTY IN INTEREST

The real party in interest is NEC Electronics Corporation, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant, Appellant's legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-22, all the claims pending in the application, are set forth fully in the attached Appendix. It is noted that these are the claims submitted in the Amendment Under 37 CFR § 1.116, filed on February 26, 2004. In the Advisory Action dated March 22, 2004, the Examiner failed to indicate (e.g., Item 7 on the Advisory Action) whether the Amendment would be entered upon Appeal. Therefore, Appellants have submitted a Petition to Admit Entry of Amendment Filed Under 37 CFR §1.116, to clarify that entry of the Amendment has occurred for purpose of this Appeal.

It is also noted that the Examiner failed to list the status of the claims under Item 7 for purpose of Appeal. Therefore, the status of the claims are herein surmised by Appellants, pending clarification by the Examiner in the Examiner's Answer, since the rejection currently of record is inconsistent relative to which claims are allowed, allowable, and rejected.

As best understood, the Rejection under 35 USC §112, second paragraph, has been withdrawn, in accordance with the Interview Summary dated March 1, 2004:

"*Atroney's (sic) argument about the second paragraph of 35 U.S.C. 112 is persuasive ....*"

As best understood, claims 8-14 and 16-18 are allowed, as based on the Examiner's statements in Paragraph 5 on page 6 of the Office Action dated August 27, 2003, and claims 3-7 stand as being allowable if rewritten in independent form. However, it is noted that claims 3 and 8-10 are also listed as rejected by Rink.

As best understood, claims 1- 2, 15, and 19-20 currently stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kamioka et al. (U.S. Patent No. 5,831,951) and by the Appellants' Admitted Prior Art (APA).

Claims 21 and 22 are stated as being rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 4,950,268 to Rink et al. However, the rejection actually addresses claims 1-3, 8-10, and 22 and seemingly fails to address claim 21.

Therefore, since the final rejection seemingly considers claims 3 and 8-10 as both allowed/allowable and as rejected by Rink, Appellants again request that the Examiner clarify, in the Examiner's Answer, exactly which claims are being rejected for purpose of this Appeal.

The somewhat cryptic comment ("... *but the second isuue (sic) is the rejection 35 U.S.C. 102 (sic) is not persuasive because the Prior art on fig 8 (sic) shows all limitations of claim 1*") in the Interview Summary dated March 1, 2004, also makes it confusing which prior art rejections are considered as being maintained for purpose of this Appeal.

For purpose of this Appeal, Appellants assume that claims 1, 2, 15, and 19-22 are subject to a continuing anticipation rejection under one or more of Kamioka, APA, or Rink.

IV. STATEMENT OF AFTER-FINAL AMENDMENTS

An Amendment Under 37 CFR §1.116 was filed on February 26, 2004. Since the Examiner failed to indicate whether the Amendment would be entered for purpose of Appeal, Appellants have filed concurrently a Petition to admit entry of this Amendment, in order to ensure that the claim amendments and arguments are a part of the record for discussion in this Appeal Brief. As pointed out in the Petition, the claim amendments in that Amendment are nonsubstantive and do not touch on the merits of the rejection currently of record.

V. SUMMARY OF THE INVENTION

As described and claimed, for example by claim 1, the present invention addresses a power control circuit for a laser diode. An amplifier circuit produces at an output terminal thereof an output voltage responsive to a voltage difference between a reference voltage and a feedback voltage that is indicative of an optical power generated by the laser diode in response to a driving current flowing therethrough.

A driving circuit responds to the output voltage to control the driving current so as

to make the voltage difference small. The amplifier circuit drives the output terminal with a first time constant during a steady operation and with a second time constant that is smaller than the first time constant upon initiation and before the steady operation.

Exemplary advantages provided by the claimed combination of the present invention include the feature that the operation mode can be quickly shifted and the feature that stabilization in the optical output of a laser diode can be improved (e.g., see page 8, lines 1-14 and 25-28; page 9, lines 1-9 and 21-27; page 10, lines 1-8; page 12, lines 1-27; and page 13, lines 1-3 of the present application).

The conventional systems, such as those discussed in APA, Kamioka, and Rind, do not have such a structure, and fail to provide for such an operation.

Independent claims 15 and 21 claim features of the present invention in different wording.

VI. ISSUES PRESENTED FOR REVIEW

Appellant presents the single following issue for review by the Board of Patent Appeals and Interferences:

Anticipation

Whether the rejections, based on Kamioka, APA, or Rink, are proper under 35 U.S.C. § 102(b) for claims 1, 2, 15, and 19-22, when it is clear that one of ordinary skill in the art could not agree that these references show two time constants in accordance with the plain meaning of the context and description of the claim language.

VII. GROUPING OF THE CLAIMS

As supported by the following arguments, independent claims 1 and 15 stand or fall together because of the similarity of the wording in the independent claims describing the scope of coverage as a broad concept. Independent claim 21 stands or falls alone because of its different wording.

Each of the dependent claims 2, 19, 20, and 22 is patentably distinct from the independent claims from which they depend. More specifically, dependent claims 2, 19, and 20 are patentably distinct from independent claim 1 by reason that the concepts described therein are distinctly different from each other and from the concepts of the independent claim and are not interrelated. Dependent claim 22 is patentably distinct from independent claim 21 by reason of the description therein of the additional components.

VIII. ARGUMENTS

THE EXAMINER'S POSITION ON ANTICIPATION

The Examiner's position on anticipation is represented in the prior art rejection in the Office Action dated August 28, 2003, and the Examiner's statements to the attachment to the Advisory Action dated March 1, 2004.

More specifically, working in reverse chronological order, in the Advisory Action, the Examiner states:

"Applicant's argument is not persuasive because the claim language does not support for the applicant's argument (sic). Nothing in claim (sic) recites about the using for reading or writing as applicant's (page 10, third and fourth paragraph) so Kamioka patent (sic) recites all limitations of a power control circuit with first constant and second constant. Respect (sic) to applicant's argument about the rejection based on APA, applicant's argument is not persuasive because the claim does not support for applicant's argument (sic). The claim does not reicte (sic) how to create a first time constant and second time contant (sic). In fig. 8 shows (sic) that RC circuit and switch S W0 (sic) at high and low cause the first time constand (sic) and second time constant. Therefore, the claims are not patentable distinct (sic) over the Kamioka patent or APA."

In the Office Action dated August 27, 2003, the Examiner states:

"Regarding to claims 1, 2, 15, and 19-20, Kamioka et al. disclosed in fig. 5 a control circuit for laser diode, comprising: an amplifier circuit producing at an output terminal and feedback voltage that is indicative of an optical power generated by laser diode (not shown) in response to a driving current flowing there through; a driving circuit responding to output voltage to control driving current so as to make voltage difference

small; amplifier circuit driving output terminal with a first time constant during a steady operation and with a second time second time (sic) constant (See column 4, line 53-58).

Regarding to claim 1, 2, 15, and 19-20, prior art discloses on fig. 8 read on limitations of claims (sic).

Regarding to claims 1, 2, 8, and 9, Rink disclosed in fig. 2 a control circuit for laser diode, comprising: an amplifier circuit (64) producing at an output terminal and feedback voltage that is indicative of an optical power via PD (57) generated by laser diode (not shown) in response to a driving current flowing there through; a driving circuit responding to output voltage to control driving current so as to make voltage difference small; a second amplifier circuit (61) producing at a second output terminal. (See Fig. below). It is inherent that amplifier circuit driving output terminal with a first time constant during a steady operation (created by two switch C2) and with second time second time (sic) constant because, when switch(67) is off (open) the gain the operation amplifier (66) is determined by the resistor (63) and capacitor (66), the RC operating to suppress overshoot and/or undershoot of the signal, thus amplifier (64) drives the terminal with a first time constant. When switch (67) is on (close) and switch (59) open then the operation of amplifier (64) functions as a voltage follower in spite of the resistor (63) and capacitor (66). Thus, amplifier 64 drives with a second time constant that is smaller the first time constant (sic). (See Fig. below);

Regarding to claim 3, and 10 Rink discloses at least one of first and second amplifier circuit includes an operational amplifer (64 and 61), a capacitor (66) coupled between output and input ends of operation amplifier and first switch (67) coupled in parallel to capacitor (66) (See column 6, line 28-53 and Fig. below)

Regarding to claim 22, Rink discloses amplifier (49) circuit further a first resistor (a), a second resistor (51) coupled in parallel to capacitor (See fig. below)."

In the Response to Arguments (e.g., Paragraph 6 of the Office Action, beginning on page 6), the Examiner further alleges:

"*Claims 1, 15, and 21 are confusing, vague, and indefinite. For example, claims 1, 15 and 21 recite amplifier circuit, feed back voltage, driving circuit without any recitation of limitations in order to make voltage difference small and amplifier circuit driving said output terminal with a first time constant during a steady operation and with a second time constant that is smaller than said first time constant upon initiation and before steady operation. The claim is not clear so examiner gives the broadest interpretation of the claim. Kamioka et al. or Rink or Prior art disclose the amplifier circuit, feed back voltage, driving circuit. Rink shows an integrator 64.*"

Thus, although Appellants find it somewhat difficult to follow the Examiner's

statements or the underlying reasoning, it appears that, based on the final paragraph above, the Examiner considers that there is a lower standard of review appropriate when an Examiner considers a claim to be "confusing, vague, and indefinite".

It also appears that the Examiner considers that specific circuits in Kamioka, APA, and/or Rink satisfies all the claim limitations of claims 1, 2, 15, and 19-22 and, possibly, claims 3, 8, 9, and 10, as these limitations would be interpreted by one of ordinary skill in the art.

D. APPELLANTS' POSITION ON ANTICIPATION

1. IN GENERAL

First, the Examiner's position is flawed as a matter of law.

Appellants first submit that the Examiner's statement ("*The claim is not clear so examiner gives the broadest interpretation of the claim.*") indicates a basic confusion on understanding of the Examiner's mandate to give the broadest reasonable interpretation (e.g., MPEP § 2111) to claim language.

This broad interpretation is not, however, contingent upon a perceived standard of "clearness" and does have a constraint. That is, as clearly stated in MPEP § 2111, the reasonably broad interpretation "... *must also be consistent with the interpretation that those skilled in the art would reach*".

As Appellants keep repeating on the record, one of ordinary skill in the art would not agree with the Examiner that the circuits to which the Examiner points meet the plain meaning of the claim language. Moreover, it is submitted that the above-mentioned Interview Summary states that the indefiniteness rejection has been removed.

Second, in order to satisfy the legal requirement for anticipation, the prior art reference must teach every single element of the claimed invention (e.g., see MPEP § 2131). This requirement is particularly significant in the rejection of record since, regardless of any

other similarities and as Appellants have repeatedly asserted on the record, the circuits to which the Examiner points to in Kamioka and Rink do not control current in a laser diode.

Third, the Examiner's remarks in the Advisory Action seem to suggest that the Examiner considers that the claim language must reflect the technical arguments of an Applicant during prosecution. Appellants submit that no such legal requirement exists, since the claim language must be interpreted as one of ordinary skill in the art would interpret this language, not, as the Examiner seems to require, that any and all words used during technical arguments must appear in the claims in order to have any technical persuasive benefit.

Therefore, in view of the above observations, Appellant submits that the prior art rejections clearly fail to meet the Examiner's initial burden by failing to abide by the proper legal standards, as discussed above.

Second, the Examiner's position is flawed as a matter of fact.

As pointed out on the record by Appellants and because the rejection currently of record fails to follow the proper legal standards described above, Appellants submit that one of ordinary skill in the art would readily disagree that the rejections currently of record fail to meet the Examiner's initial burden. Details for each currently rejected claim is provided below, as can best be deciphered from the rejection currently of record.

Independent Claims 1 and 15

Appellants have repeatedly pointed out that Kamioka Figure 5 addresses a binarization circuit related to the processing of data read off the disk, not a power circuit controlling the power in a laser diode, as required by the plain meaning of the claim language. Therefore, the reference to two time constants at lines 55-58 of column 4 is irrelevant, since the feedback loop is not related to controlling the power in a diode and the existence of two time constants does not overcome the basic deficiency that Figure 5 is not a feedback loop for power in a laser diode. Appellants submit that the Examiner is not entitled to simply ignore the plain meaning of the environment of the circuit of Kamioka.

Relative to the rejection based on Figure 8 (e.g., APA) of the specification, as clearly described at line 15 of page 4 through line 6 of page 5, the effect of switch SW0 is the deactivation of the command signal from the DAC and not for switching in a second time constant, as alleged in the rejection of record. As clearly described, the switching to ground disables the amplifier 4 output as being a contributor to the control of the power for the laser diode. Again, the Examiner cannot simply ignore the plain meaning of the description of the operation of this circuit.

Relative to the rejection based on Rink and as best understood, the Examiner alleges that Figures 2 and 3 of Rink anticipate the present invention as defined by various claims. However, similar to the comments above for Kamioka, the Examiner's evaluation must be consistent with the plain meaning of the language of the claims and prior art references, as interpreted by one of ordinary skill in the art.

Applicants submit that one of ordinary skill in the art would be quite confused as to how the Examiner is attempting to apply these two figures so that any of the claims in the present Application read upon them.

First, it is noted that Figure 2 is described at lines 3-7 of column 3 as demonstrating a "... *temperature safety circuit that senses an overtemperature condition in the laser system and shuts off power to the laser power supply*". According to the description beginning at lines 64 of column 5, this Figure 2 is not related to a control circuit for power of a laser diode, except that, upon sensing an overtemperature, using infrared photodetector 57, this circuit pulls down AND input 32R, which, in turn chops "... *the duration of the next successive laser pulse in response to the previous temperature level*".

Relative to the Examiner's description that C_2 causes the amplifier 64 to operate with two separate time constants, Applicants submit that, as clearly described at lines 46-48 of column 6, the purpose of the two switches controlled by C_2 is not to provide two time constants but to reset the integrator formed by capacitor 66 with op amp 64 so as "... *to reset the integration product to zero prior to each laser pulse*."

Therefore, to one of ordinary skill in the art, the circuit shown in Figure 2 does not have two operational time constants, since the reset period between laser pulses would not be a "time constant", as that term is understood by one of ordinary skill in the art. If anything, one of ordinary skill in the art would consider the shorting out of the capacitor as being a transient during which time the laser diode is not operating and would also consider that the integrator circuit 64,66 is also not operating.

Hence, turning to the clear language of the independent claims, there is no teaching or suggestion in Rink of: "...said amplifier circuit driving said output terminal with a first time constant during a steady operation and with a second time constant that is smaller than said first time constant upon initiation and before said steady operation", as required by claims 1 and 15.

Independent Claim 21

Although the rejection currently of record fails to explicitly address claim 21, as best understood, Appellants suspect that the Examiner might be intending that this claim be rejected as anticipated by Figure 2 of Rink, even though the wording of the rejection refers to claims 1, 2, 8, and 9, rather than claim 21.

However, if such is the intent of the Examiner, it is suggested that this rejection needs additional clarification prior to proceeding to appeal. Along this line, it is noted that the integrator formed by capacitor 66 does not function as a feedback control to make the input voltage small, as required by the plain meaning of the claim language. Rather, the integrator output is provided to an input into the threshold detector formed by amplifier 68 and resistor 70 and would control, at most, the pulse width of the next laser pulse, rather than the driving current itself and, even that occurs only if the integrator output exceeds a threshold.

Relative to the rejection for claim 22, in which the Examiner relies upon Figure 3 of Rink, it is noted that this figure does not illustrate the amplifier circuit of Figure 2, so that a

Rink, it is noted that this figure does not illustrate the amplifier circuit of Figure 2, so that a rejection of a claim depending from claim 21 is inherently improper.

It is also noted that, to one of ordinary skill in the art, Figure 3 of Rink fails to show a "... a first resistor coupled to an input end of said operational amplifier; and a second switch coupled to said input end of said operational amplifier through said first resistor ", as required by the plain meaning of the claim language.

Thus, Applicants submit that one of ordinary skill in the art would not consider that either Figure 2 or Figure 3 of Rink teaches or suggests the present invention, as defined by the independent claims.

In summary, Appellants submit that the rejection currently of record improperly attempts to provide an overly-broad interpretation to the prior art references by simply ignoring the plain meaning of these references, as would be understood by one of ordinary skill in the art. That is, for example, the binarization circuit of Kamioka Figure 5 does not get converted into a current control circuit for a laser diode by reason of the Examiner's mandate to make a "reasonably broad interpretation", since one of ordinary skill would not agree that the binarization circuit controls the current in the laser diode of the Kamioka device.

Therefore, Appellants submit that the rejection currently of record for the independent claims 1, 15, and 21 does not contain rejections that meet the Examiner's initial burden for a *prima facie* rejection under 35 USC §102.

Dependent Claims 2, 3, 9,10, 19, 20 and 22

Dependent claims 2, 19, and 20 are understood as being rejected by Kamioka and by APA. However, it is noted that the rejection currently of record fails to specify how lines 53-58 of column 4 of Kamioka or anything in the APA could possibly address the plain meaning of these claims. Therefore, it is submitted that the Examiner has failed to meet his initial burden.

3 and 10) as based on Rink Relative to claim 2, there is some hint that the Examiner seems to be attempting to consider the time between pulses as being the second, shorter time constant. However, such interpretation would be inconsistent with the plain meaning of the language of claim 2, since the amplifer would clearly not be driving the diode between pulses.

Relative to claims 3, 8, 9, and 10, it is noted that the Examiner seems to consider these claims are actually allowable (e.g., see Paragraphs 4 and 5 on page 6). Therefore, it is requested that the Examiner clarify the intended status of these claims for purpose of Appeal and clarify specifically how Rink is being interpreted so as to anticipate these claims.

Relative to the rejection for claim 22, in which the Examiner relies upon Figure 3 of Rink, it is noted that this figure does not illustrate the amplifier circuit of Figure 2, so that a rejection of a claim depending from claim 21 is inherently improper.

IX. CONCLUSION

In view of the foregoing, Appellants submit that claims 1-22, all the claims presently pending in the application, are clearly and patentably distinct form the prior art of record and in condition for allowance. Thus, the Board is respectfully requested to remove all rejections of claims 1-22.

Please charge any deficiencies and/or credit any overpayments necessary to enter this paper to Attorney's Deposit Account number 50-0481.

Respectfully submitted,

Dated: 4/26/04

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APPENDIX

1. (Previously presented) A power control circuit for a laser diode, comprising:

an amplifier circuit producing at an output terminal thereof an output voltage responsive to a voltage difference between a reference voltage and a feedback voltage that is indicative of an optical power generated by said laser diode in response to a driving current flowing therethrough; and

a driving circuit responding to said output voltage to control said driving current so as to make said voltage difference small,

said amplifier circuit driving said output terminal with a first time constant during a steady operation and with a second time constant that is smaller than said first time constant upon initiation and before said steady operation.

2. (Original claim) The circuit according to claim 1, wherein said second time constant is derived by increasing a driving ability of said amplifier circuit upon said initiation larger than that during said steady operation.

3. (Original claim) The circuit according to claim 1, wherein said amplifier circuit includes an operational amplifier, a capacitor coupled between output and input ends of said operational amplifier, and a first switch coupled in parallel to said capacitor, said first switch being turned OFF during said steady operation and ON upon said initiation.

4. (Original claim) The circuit according to claim 3, wherein said amplifier circuit further includes a first resistor, a second resistor coupled in parallel to said capacitor, and a second switch coupled to said input end of said operational amplifier through said first resistor, said second switch being turned ON during said steady operation and OFF upon said initiation.

5. (Original claim) The circuit according to claim 3, wherein said amplifier circuit further includes a reference voltage generation circuit coupled to said amplifier circuit, generating first and second reference voltages and providing said amplifier circuit with said first reference voltage as said reference voltage during said steady operation and with said second reference voltage that is higher than said first reference voltage as said reference voltage upon said initiation.

6. (Previously presented) The circuit according to claim 5, wherein said amplifier circuit further includes a third switch coupled to said capacitor, forming an electrical path between said input end of said operational amplifier and said capacitor during said steady operation and providing said capacitor with said first reference voltage upon said initiation.

7. (Original claim) The circuit according to claim 4, wherein said amplifier circuit further includes a fourth switch coupled between said input end of said operational amplifier and said capacitor, forming an electrical path between said input end of said operational amplifier and said capacitor during said steady operation and providing said capacitor with said feedback voltage without said electrical path upon said initiation.

8. (Previously presented) A power control circuit for a laser diode, comprising:

a first amplifier circuit producing, when activated, at a first output terminal thereof a first output voltage responsive to a first voltage difference between a first reference voltage and a feedback voltage that is indicative of an optical power generated by said laser diode in response to a driving current flowing there through;

a second amplifier circuit producing, when activated, at a second output terminal thereof a second output voltage responsive to a second voltage difference between a second reference voltage and said feedback voltage; and

a driving circuit responding to an activated one of said first and second output

voltage to control said driving current so as to make a corresponding one of said first and second voltage difference small, respectively,

at least one of said first and second amplifier circuits driving one of said first and second output terminals with a first time constant during a steady operation and with a second time constant that is smaller than said first time constant upon initiation and before said steady operation.

9. (Original claim) The circuit according claim 8, wherein said second time constant is derived by increasing a driving ability of said amplifier upon said initiation larger than that during said steady operation.

10. (Original claim) The circuit according claim 8, wherein at least one of said first and second amplifier circuits includes an operational amplifier, a capacitor coupled between output and input ends of said operational amplifier, and a first switch coupled in parallel to said capacitor, said first switch being turned OFF during said steady operation and ON upon said initiation.

11. (Previously presented) The circuit according claim 10, wherein at least one of said first and second amplifier circuits further includes a first resistor, a second resistor coupled in parallel to said capacitor, and a second switch coupled to said input end of said operational amplifier through said first resistor, said second switch being turned ON during said steady operation and OFF upon said initiation.

12. (Original claim) The circuit according claim 11, wherein at least one of said first and second amplifier circuits further includes a reference voltage generation circuit generating first and second reference voltages and providing said operational amplifier with said first

reference voltage during said steady operation and with said second reference voltage that is higher than said first reference voltage as said reference voltage upon initiation.

13. (Previously presented) The circuit according claim 11, wherein at least one of said first and second amplifier circuits further includes a third switch coupled to said capacitor, forming an electrical path between said input end of said operational amplifier and said capacitor during said steady operation and providing said capacitor with said first reference voltage upon said initiation.

14. (Original claim) The circuit according claim 12, wherein at least one of said first and second amplifier circuits further includes a fourth switch coupled between said input end of said operational amplifier and said capacitor, forming an electrical path between said input end of said operational amplifier and said capacitor during said steady operation and providing said capacitor with said feedback voltage without said electrical path upon said initiation.

15. (Previously presented) A power control circuit for a laser diode, comprising:

an amplifier circuit producing at an output terminal thereof an output voltage responsive to a voltage difference between a reference voltage and a feedback voltage that is indicative of an optical power generated by said laser diode in response to a driving current flowing therethrough; and

a driving circuit responding to said output voltage to control said driving current so as to make said voltage difference small,

wherein said output voltage comprises a steady operation period of time and an initiation period of time prior to said steady operation period of time,

wherein said driving current flows through said laser diode during both said steady operation period of time and said initiation period of time, and

wherein said amplifier circuit drives said output terminal with a first time constant during said steady operation period of time and with a second time constant, which is smaller than said first time constant, during said initiation period of time.

16. (Previously presented) The circuit according to claim 8, wherein each of said first and second output voltages comprises a steady operation period of time and an initiation period of time prior to said steady operation period of time.

17. (Previously presented) The circuit according to claim 16, wherein said driving current flows through said laser diode during both said steady operation period of time and said initiation period of time.

18. (Previously presented) The circuit according to claim 16, wherein at least one of said first and second amplifier circuits drives an associated one of said first and second output terminals with a first time constant during said steady operation period of time and with a second time constant, which is smaller than said first time constant, during said initiation period of time.

19. (Previously presented) The circuit according to claim 1, wherein said output voltage comprises a steady operation period of time and an initiation period of time prior to said steady operation period of time.

20. (Previously presented) The circuit according to claim 1, wherein said driving current flows through said laser diode during both said steady operation period of time and said initiation period of time.

21. (Previously presented) A power control circuit for a laser diode, comprising:

an amplifier circuit producing at an output terminal thereof an output voltage responsive to a voltage difference between a reference voltage and a feedback voltage that is indicative of an optical power generated by said laser diode in response to a driving current flowing therethrough, said amplifier circuit including an operational amplifier;

a driving circuit responding to said output voltage to control said driving current so as to make said voltage difference small;

a capacitor coupled between input and output ends of said operational amplifier; and

a first switch coupled in parallel to said capacitor.

22. (Previously presented) The power control circuit according to claim 21, further comprising:

a first resistor coupled to an input end of said operational amplifier; and

a second switch coupled to said input end of said operational amplifier through said first resistor.